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Anton Rozen

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EXAMINER

HERNANDEZ, MANUEL J

ART UNIT

PAPER NUMBER

2858

NOTIFICATION DATE

DELIVERY MODE

10/29/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/595,908	Applicant(s) ROZEN ET AL.	
	Examiner MANUEL HERNANDEZ	Art Unit 2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. <u> / / </u> |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>6/16/2009</u> . | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Receipt is acknowledged of the amendment and IDS filed on 6/16/2009, which have been entered in the file. Claims 1-30 are pending.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Claim 1 reads, "a regulator; wherein wherein the memory..." This should be changed to read "a regulator; wherein the memory..." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Art Unit: 2858

5. Claims 1-4, 6-8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) in view of Borkar et al (US 6,484,265).

Regarding claims 1 and 9, Brown teaches a device for regulating a voltage supply to a semiconductor device (Abstract), said device comprising:

a memory (Figure 2, 24) for storing a performance range (column 3, lines 23-33), wherein said performance range is associated with a respective supply voltage (column 3, lines 15-19) and said performance range has a performance limit of the semiconductor device associated therewith ("optimum operating performance", column 3, lines 33-34);

a measuring function for measuring a performance of said semiconductor device (column 3, lines 52-60, column 4, lines 14-18);

a reference circuit (Figure 2, 39; i.e. which measures a performance of said semiconductor device; column 3, lines 52-60; column 4, lines 14-18); and

a regulator (Figure 1, 16); wherein

the memory, the reference circuit and the regulator are arranged to determine a lowest supply voltage (column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance ("optimum operating performance", column 3, lines 33-34) of the semiconductor device at a given operational frequency (column 3, lines 56-57).

Brown fails to disclose a plurality of performance ranges, and the modification of supply voltage if a measured performance is not within a performance range.

Borkar et al teach a plurality of performance ranges (column 4, lines 53-56; column 12, lines 29-32), wherein each performance range of said plurality of

Art Unit: 2858

performance ranges is associated with a respective different supply voltage (column 4, lines 53-56; column 12, line 35 – column 13, line 38) and the modification of the supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to said semiconductor device (column 13, lines 2-38, column 4, lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Brown for regulating a voltage supply to a semiconductor device to include a plurality of performance ranges and the modification of the supply voltage if measured performance is not within a performance range as described by Borkar et al. One would have been motivated to include the plurality of performance ranges and the modification of the supply voltage to control various parameters of the semiconductor device, providing for an increase in performance, a reduced power consumption, and prevention of processor overheating. (Borkar, column 1, lines 48-56, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 2, Brown as modified by Borkar et al disclose a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said performance limits stored in the memory are based on two parameters, the first parameter being current resistance drop value and the second parameter being an accuracy of the regulator.

One of ordinary skill, however, would recognize the need to take into account parameters such as the current resistance drop value and the accuracy of the regulator

Art Unit: 2858

when setting the performance limits. For instance, if the current resistance drop value is not taken into account, then the semiconductor device would not receive sufficient voltage. If the accuracy of the regulator is not taken into account, then the semiconductor device would not receive the desired voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to program the memory based on these two parameters. One would have been motivated to program the memory based at least on these parameters since the semiconductor device would fail to operate correctly if these two parameters were not taken into consideration at the time the memory was programmed.

Regarding claim 3, Brown as modified by Borkar et al teaches said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of the semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 25-28).

Regarding claim 4, Brown as modified by Borkar et al teaches said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance limit said regulator is arranged to increase said voltage supplied to the semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 6, Brown as modified by Borkar et al discloses said measuring function is arranged to measure said performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 7, Brown as modified by Borkar et al disclose a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said plurality of performance ranges are arranged to include a performance guard margin to compensate for differences between said measured performance of said reference circuit and an actual performance of a complete integrated circuit.

One of ordinary skill in the art, however, would recognize the need to compensate for differences between a measured performance of the reference circuit and the actual performance of an integrated circuit. It is well known in the art that variations exist in semiconductor devices. If the differences between said measured performance of said reference circuit and an actual performance are not taken into account, then the semiconductor device would not receive the appropriate voltage from the voltage regulator.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a performance guard margin. One would have been motivated to include the performance guard margin to compensate for different characteristics amongst different transistors in an semiconductor device (Borkar, column 9, lines 25-29) thereby providing means to reduce mismatches between transistors of different domains (Borkar, column 10, lines 19-42) and ultimately to control various parameters

Art Unit: 2858

of the semiconductor device, providing for an increase in performance, a reduced power consumption, and prevention of processor overheating. (column 1, lines 48-56, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 8, Brown as modified by Borkar et al discloses a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of said performance of an integrated circuit (Brown, column 4, lines 14-18).

6. Claims 5 and 10-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) and Borkar et al (US 6,484,265) in view of Bonnett (US 6,996,730).

Regarding claim 10, Brown and Borkar et al teach the device for regulating a voltage supply to a semiconductor device as described above but fail to disclose a plurality of process temperature compensation voltages and the modification of voltage supply with respect to a change in operational frequency.

However, one of ordinary skill in the art would recognize that Borkar et al disclose a plurality of process temperature compensation voltages (Borkar, column 2, lines 1-3; column 4, lines 53-56; column 13, lines 35-38) for a given setting, amongst them a clock signal. Bonnett more specifically discloses said respective process temperature compensation voltage values (Bonnett, column 6, line 47 – column 7, line 3) are associated with a respective operational frequency for said semiconductor device, such that if said operational frequency of said semiconductor device changes to

Art Unit: 2858

a new operational frequency, said supply voltage is modified by said regulator to substantially a same value as said process temperature compensation voltage value associated with said new operation frequency (Bonnett, column 2, lines 27-45; column 4, lines 4-21).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown and Borkar et al. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (Bonnett, column 2, lines 16-20).

Regarding claim 5, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 11, Brown and Borkar et al as modified by Bonnett teaches each process temperature compensation voltage value associated with a respective operational frequency is determined from a plurality of performance ranges stored in said memory wherein said respective performance ranges are associated with a respective supply voltage (Bonnett, column 4, Table 1).

Art Unit: 2858

Regarding claim 12, Brown and Borkar et al as modified by Bonnett teaches said regulator is arranged to modify said supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to the semiconductor device (Brown, column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43) for a given frequency (Bonnett, column 4, Table 1).

Regarding claim 13, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 14, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 15, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to

Art Unit: 2858

increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 16, Brown and Borkar et al as modified by Bonnett teaches said measuring function is arranged to measure the performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 17, Brown, Borkar et al and Bonnett teach a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said plurality of performance ranges are arranged to include a performance guard margin to compensate for differences between said measured performance of said reference circuit and an actual performance of said semiconductor device.

One of ordinary skill in the art, however, would recognize the need to compensate for differences between a measured performance of the reference circuit and the actual performance of an integrated circuit. It is well known in the art that variations exist in semiconductor devices. If the differences between said measured performance of said reference circuit and an actual performance are not taken into account, then the semiconductor device would not receive the appropriate voltage from the voltage regulator.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a performance guard margin. One would have been motivated to include the performance guard margin to compensate for different characteristics amongst different transistors in an semiconductor device (Borkar, column 9, lines 25-29)

Art Unit: 2858

thereby providing means to reduce mismatches between transistors of different domains (Borkar, column 10, lines 19-42) and ultimately to control various parameters of the semiconductor device, including performance, power consumption, and temperature (Borkar, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 18, Brown and Borkar et al as modified by Bonnett teaches a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of the performance of the semiconductor device (Brown, column 4, lines 14-18).

Regarding claim 19, Brown and Borkar et al teach a method for regulating a voltage supply to a semiconductor device as described above, but fail to disclose a plurality of process temperature compensation voltages and the modification of voltage supply with respect to a change in operational frequency.

Bonnet discloses said step of storing comprises storing a plurality of process temperature compensation voltage values, wherein respective process temperature compensation voltage values are associated with a respective operational frequency for said semiconductor device (column 5, lines 15-22, lines 25-28); and

said step of modifying comprises modifying a supply voltage to said semiconductor device if an operational frequency of said semiconductor device changes to a new operational frequency, wherein said supply voltage is modified to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency (column 2, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown and Borkar et al. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (column 2, lines 16-20).

Regarding claims 20 and 30, Brown as modified by Borkar et al and Bonnet teach a device for regulating a voltage supply to a semiconductor device (Brown, Abstract) comprising:

a memory for storing a plurality of process temperature compensation voltage values, wherein each of said plurality process temperature compensation voltage values are respectively associated with a different operational frequency for said semiconductor device (Bonnett, column 5, lines 15-22, lines 25-28; Borkar, column 2, lines 1-3; column 4, lines 34-43 and lines 53-56; column 12, line 35 – column 13, line 38; column 13, lines 35-38); and

a regulator for modifying said supply voltage to said semiconductor device if said operational frequency of said semiconductor device changes to a new operational frequency (Bonnett, column 2, lines 36-39), and modify said supply voltage to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency (Bonnett, column 2, lines 36-39).

the memory (Brown, Figure 2, 24) stores a performance limit (Brown, “optimum operating performance”, column 3, lines 33-34) of the semiconductor device, the

Art Unit: 2858

memory, a reference circuit (Brown, Figure 2, 39) and the regulator being arranged to determine a lowest supply voltage (Brown, column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance (Brown, "optimum operating performance", column 3, lines 33-34) of the semiconductor device at a given operational frequency (Brown, column 3, lines 56-57).

Regarding claim 21, Brown as modified by Borkar et al and Bonnett teach a device for regulating a voltage supply to a semiconductor device as described above (see claim 2).

Regarding claim 22, Brown as modified by Borkar et al and Bonnett teach the device for regulating a voltage supply to a semiconductor device as described above further teaching each process temperature compensation voltage value associated with a respective operational frequency is determined from a plurality of performance ranges (Borkar, column 12, lines 29-32) stored in said memory wherein said respective performance ranges are associated with a respective supply voltage (Borkar, column 12, lines 29-32).

Regarding claim 23, Brown as modified by Borkar et al and Bonnett teach a measuring function for measuring the performance of the semiconductor device (Borkar, column 10, lines 51-53, 34-66), wherein said regulator is arranged to modify said supply voltage to said semiconductor device if a measured performance of the semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to said semiconductor device (Borkar, column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43) for a given frequency (Borkar, column 4, lines 53-56).

Regarding claim 24, Brown as modified by Borkar et al and Bonnett teach said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 25-28).

Regarding claim 25, Brown as modified by Borkar et al and Bonnett teach said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 26, Brown as modified by Borkar et al and Bonnett teach said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 27 Brown as modified by Borkar et al and Bonnett teach said measuring function is arranged to measure the performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 28, Brown as modified by Borkar et al and Bonnett teach the device for regulating a voltage supply to a semiconductor device as described above (see claim 7).

Regarding claim 29, Brown and Bonnett as modified by Borkar et al discloses a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of a performance of the semiconductor device (Brown, column 4, lines 14-18).

Response to Arguments

7. Applicant's arguments, see page 3, lines 13-22, page 4, lines 20-28, page 5, lines 13-24, and page 6, lines 28-30 of Remarks, filed 6/16/2009, with respect to claims 1, 9, 20, and 30 have been fully considered and are persuasive. The rejection of claims 1, 9, 20, and 30 have been withdrawn.

8. Applicant argues that Brown and Borkar et al fail to teach the storage of multiple supply voltage values that each has a performance range associated therewith. Borkar et al states that a supply voltage may have performance ratings determined and stored in a memory (Borkar, column 12, lines 29-33), and to maintain a performance rating different parameters may be adjusted (Borkar, column 4, lines 53-56; column 12, lines 35-61), thus creating a plurality of performance ranges associated with a certain supply voltage and the voltage values associated with operational frequencies.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2858

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MANUEL HERNANDEZ whose telephone number is (571)270-7916. The examiner can normally be reached on 5/4/9 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Assouad can be reached on 571-272-2210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2858

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M.H./

10/27/09

/Patrick J Assouad/

Supervisory Patent Examiner, Art Unit 2858